REMARKS

Claims 1 to 21 were pending in the Application at the time of examination. The Examiner objected to the Specification. The Examiner provisionally rejected Claims 1 to 21 under the judicially created doctrine of obviousness-type double patenting. The Examiner rejected Claims 1 to 21 under 35 U.S.C. 112, second paragraph. The Examiner rejected Claims 1 to 21 under 35 U.S.C. 103(a) as obvious over the Dukach et al. reference (US 6,609,159 B1) in view of the Woodring et al reference (US 6,519,686 B2).

Applicants have amended the description to correct typographical errors. Applicants have Amended Claims 1, 7 and 21. Consequently, Claims 1 to 21 remain in the Application.

OBJECTIONS TO THE SPECIFICATION

The Examiner objected to the Specification.

As shown above Applicants have amended the Specification to correct a typographical error at page 11, line 3.

In light of the Amendment to the Specification, Applicants respectfully request the Examiner withdraw the objection to the Specification.

PROVISIONAL REJECTION OF CLAIMS 1 TO 21 UNDER THE JUDICAILLY CREATED DOCTRINE OF OBVIOUSNESS-TYPE DOUBLE PATENTING

The Examiner provisionally rejected Claims 1 to 21 under the judicially created doctrine of obviousness-type double patenting.

The Examiner states:

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> Claims 1-21 are **provisionally** rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-21 of **copending** application serial number 09/991569. (Office Action, page 2, emphasis added.)

Accordingly, Applicants respectfully request that the provisional rejection be held in abeyance until the conflicting claims have in fact been patented.

REJECTION OF CLAIMS 1 TO 21 UNDER 35 U.S.C. 112, SECOND PARAGRAPGH

The Examiner rejected Claims 1 to 21 under 35 U.S.C. 112, second paragraph.

Applicants first note that page 8, lines 10 to 18 of Applicants Specification reads as follows:

> In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

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Applicants respectfully submit that the elements of Applicants Claims are all within the capability of one of skill in the art to comprehend and employ by various methods.

In addition page 9, line 15 to page 12, line 11, reads as shown below, with emphasis added, and, along with FIG.s 4 and 5 describes in some detail one embodiment of Applicants' invention:

> The present invention relies on the concept of interposition of shared objects. **For example, dynamic libraries allow a symbol to be interposed so that if more than one symbol exist, the first symbol takes precedence over all other symbols.** The environment variable LD_PRELOAD can be used to load shared objects before any other dependencies are loaded. The Speed Library uses this concept to interpose functions that will be discussed in more details below.
>
> **Speed Library interposition is needed on both the server and the client applications. This interposition allows existing client-server applications to transparently use the library.** For example, on the server side, LD_PRELOAD may be used to load the shared library LIBSPEEDUP_SERVER.SO. On the client side, LD_PRELOAD may be used to load LIBSPEEDUP_CLIENT.SO.
>
> FIG. 4 is a block diagram illustrating an interprocess communication using a Speed Library according to a specific embodiment of the present invention. A process 402 communicates with another process 404 through doors 406 and 408 and mapped memory 410. Each process 402, 404 opens a TCP socket 412, 414 respectively, which is associated with a socket library (not shown). **Through interposition, process calls for the socket library are intercepted and redirected to the Speed Library (not shown) that is associated with a door IPC mechanism.** The Speed Library enables process 402 to communicate data

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availability, or synchronization signals 426, with process 404 via doors 406 and 408. Each process transfer data through the mapped memory 410.

For example, when process 402 opens socket 412 to read data from process 404 via socket 414, the read calls 416 are interposed with the Speed Library that enables doors 406 and 408. The Speed Library enables processes 402 and 404 communicate synchronization signals via the doors 406 and 408 through kernel 418. **The mapped memory 410 enables data to transfer from process 404 to process 402 based on the synchronization signals without interfering with the kernel 418.** When process 402 opens socket 412 to write data through socket 414 to process 404, the write calls 420 are interposed with the Speed Library that enables doors 406 and 408. The Speed Library enables processes 402 and 404 communicate synchronization signals via the doors 406 and 408 through kernel 418. The mapped memory 410 enables data to transfer from process 404 to process 402 based on the synchronization signals without interfering with the kernel 418. Both processes 402 and 404 are represented in the user space 422 while the kernel 418 is represented in the kernel space 424. Thus, the sockets 402 and 404 virtually communicate (represented by line 426) while the data and synchronization signals are actually transferred through the mapped memory 410 and doors 406, 408 respectively enabled by the Speed Library.

FIG. 5 is a flow diagram illustrating a method for moving data between a first process and a second process according to a specific embodiment of the present invention. **In a first block 502, a second shared library, such as a Speed Library, is associated with a process through interposition. In block 504, a process call for a symbol in a first library, for example a TCP socket library, is intercepted by the interposer. The interposer in turn redirects the call for a corresponding symbol in the second shared library in step 506.** The corresponding symbol enables a door for each process. The processes then communicate synchronizing signals through the doors in block 508 and transfer data through a mapped memory in block 510 based on the synchronizing signals in block 508.

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> **Even tough the symbols are interposed, the TCP socket client-server semantics are not changed. Data and synchronizing signals are exchanged between processes.** For example, a server process establishes a server socket and listens on this socket. The client process connects to this port to establish a connection, starts reading and writing information as usual. But instead of flowing through the socket, the data is transferred using the mapped memory based on data availability signals traveling through the doors.
>
> In particular, data is copied into a mapped memory buffer to avoid making multiple copies of the data. A sliding window type of buffer management may be adopted. For every connection, the server process creates a mapped memory segment. This segment is divided into multiple windows. Each window is further divided into slots. The number and sizes of slots are configurable.

Applicants respectfully submit that when Applicants' Claims are read in light of Applicants Specification, the requirements of 35 U.S.C. 112, second paragraph are satisfied. In addition, Applicants have amended independent Claims 1, 7, and 21. Applicants' Claim 1, as amended, recites, with emphasis added:

> A method for moving data between processes in a computer-based system, each process calling for one or more symbols in a first library, the method comprising:
>
> associating each process with a second library, said second library comprising one or more symbols with a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal, said one or more symbols enabling data communication through a mapped memory based on said synchronization signal;

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> intercepting a call from each process for a symbol in said first library **by interposition**; and
>
> redirecting said call to a corresponding symbol in said second library **by interposition**.

Applicants Claim 7, as amended, recites, with emphasis added:

> A program storage device readable by a machine, tangibly embodying a program of instructions readable by the machine to perform a method for moving data between processes in a computer-based system, each process calling for one or more symbols in a first library, the method comprising:
>
> associating each process with a second library, said second library comprising one or more symbols with a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal, said one or more symbols enabling data communication through a mapped memory based on said synchronization signal;
>
> intercepting a call from each process for a symbol in said first library **by interposition**; and
>
> redirecting said call to a corresponding symbol in said second library **by interposition**

Applicants Claim 13 recites, with emphasis added:

> An apparatus for moving data between process in a computer-based system, the apparatus comprising:
>
> a plurality of processes;
>
> a mapped memory;
>
> a first library having one or more symbols, said plurality of processes calling for said one

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> or more symbols in said first library of symbols;
>
> a second library having one or more symbols, said one or more symbols associated with a door interprocess communication mechanism; and
>
> **an interposer** intercepting a call from a process for said one or more symbols in said first library and redirecting a call for corresponding said one or more symbols in said second library.

Applicants Claim 21, as amended, recites, with emphasis added:

> An apparatus for moving data between processes in a computer-based system, each process calling for one or more symbols in a first library, the apparatus comprising:
>
> means for associating each process with a second library, said second library comprising one or more symbols with a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal, said one or more symbols enabling data communication through a mapped memory based on said synchronization signal;
>
> **interposer** means for intercepting a call from each process for a symbol in said first library; and
>
> **interposer** means for redirecting said call to a corresponding symbol in said second library.

Applicants respectfully submit that the amendments to Claims 1, 7, 13 and 21 are fully supported by Applicants' Specification by, as one example, the text copied above.

In light of the discussion above, Applicants respectfully request the Examiner withdraw the rejection of Claims 1, 7, 13 and 21 under 35 U.S.C. 112, second paragraph.

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Claims 2 to 6 depend, directly or indirectly on Claim 1, as amended. Consequently Claims 2 to 6 include all of the features of Claim 1, as amended. Claims 8 to 12 depend, directly or indirectly on Claim 7, as amended. Consequently Claims 8 to 12 include all of the features of Claim 7, as amended. Claims 14 to 20 depend, directly or indirectly on Claim 13. Consequently Claims 14 to 20 include all of the features of Claim 13. Therefore, Applicants respectfully submit that Claims 2 to 6, 8 to 12 and 14 to 20 also meet the requirements of 35 U.S.C. 112, second paragraph and Applicants respectfully request the Examiner withdraw the rejection of Claims 2 to 6, 8 to 12 and 14 to 20 under 35 U.S.C. 112, second paragraph as well.

REJECTION OF CLAIMS 1 TO 21 UNDER 35 U.S.C. 103(a)

The Examiner rejected Claims 1 to 21 under 35 U.S.C. 103(a) as obvious over the Dukach et al. reference (US 6,609,159 B1) in view of the Woodring et al reference (US 6,519,686 B2).

Applicants have amended independent Claims 1, 7, and 21. Applicants' Claim 1, as amended, recites, with emphasis added:

> A method for moving data between processes in a computer-based system, each process calling for one or more symbols in a first library, the method comprising:
>
> associating each process with a second library, said second library comprising one or more symbols **with a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal**, said one or more symbols enabling data communication through a mapped memory based on said synchronization signal;

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intercepting a call from each process for a symbol in said first library **by interposition**; and

redirecting said call to a corresponding symbol in said second library **by interposition**.

Applicants Claim 7, as amended, recites, with emphasis added:

A program storage device readable by a machine, tangibly embodying a program of instructions readable by the machine to perform a method for moving data between processes in a computer-based system, each process calling for one or more symbols in a first library, the method comprising:

associating each process with a second library, said second library comprising one or more symbols with **a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal**, said one or more symbols enabling data communication through a mapped memory based on said synchronization signal;

intercepting a call from each process for a symbol in said first library **by interposition**; and

redirecting said call to a corresponding symbol in said second library **by interposition**

Applicants Claim 13 recites, with emphasis added:

An apparatus for moving data between process in a computer-based system, the apparatus comprising:

a plurality of processes;

a mapped memory;

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> a first library having one or more symbols, said plurality of processes calling for said one or more symbols in said first library of symbols;
>
> a second library having one or more symbols, said one or more symbols associated with a door interprocess communication mechanism; and
>
> **an interposer** intercepting a call from a process for said one or more symbols in said first library and redirecting a call for corresponding said one or more symbols in said second library.

Applicants Claim 21, as amended, recites, with emphasis added:

> An apparatus for moving data between processes in a computer-based system, each process calling for one or more symbols in a first library, the apparatus comprising:
>
> means for associating each process with a second library, said second library comprising one or more symbols with **a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal,** said one or more symbols enabling data communication through a mapped memory based on said synchronization signal;
>
> **interposer** means for intercepting a call from each process for a symbol in said first library; and
>
> **interposer** means for redirecting said call to a corresponding symbol in said second library.

As shown above, each of Applicants independent Claims 1, 7, 13 and 21, as amended, includes the recited feature of a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a

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synchronization signal and/or an interposer/interposition, or words to that effect.

The Examiner has stated, with emphasis added:

> ...Dukack (sic) teaches the invention substantially as claimed including: data (information, col 3, ln 35-42), data between processes in a computer-based system (col 6, ln 35-40/col 8, ln 37-42), one or more symbols (OS function 144, col 8, ln 55-62), the first library (the library of the OS 134, col 8 ln 52-55), process calling for one or more symbols in a first library (col 8, ln 58-62), associating each process with a second library (col 8, ln 36-37), a second library (the interposed library, col 8, ln 36-37/ln 60-65), one or more symbols of the second library(the interposed library function col 8, ln 52-65), **a door interprocess communication (file descriptor, col 3, ln 62-64/col 10, ln 33-34/ln 53-55), said door interprocess mechanism enabling each process to communication (col 15, ln1-6/col 16, ln 15-21), interprocess communication mechanism(interprocess communication links, col 8, ln 40-46),** intercepting a call from each process for a symbol in said first library(col 8, ln 58-65/col 9, ln 24-30), redirecting said call to a corresponding symbol in said second library(col 8, ln 63-65).

Applicants first note that Dukach's column 8, lines 35 to 65 reads as follows, with emphasis added:

> The back end server and the interposed library which is linked to it, are one process. The front end server is another. The OS accords each separate process its own separate subspace within the common OS space. **A given process cannot directly write to another process's sub-space, but the OS does let it communicate with another processes in the same OS space through interprocess communication links, or pipes. Such pipes are defined and only work within a given OS space defined by a given OS kernel.**

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> Although it is not mentioned elsewhere in this specification, those skilled in the computer arts will understand that the OS normally runs processes in virtual memory, i.e., a memory space larger than that which will fit in RAM at one time, and automatically swaps portions of this virtual memory space in and out of memory from and to the hard disk, as needed for current computations.
>
> As stated above, the back end server is linked to the interposed dynamically-loaded library 116. The back end server is also linked to the library of the OS 134. As is shown in FIG. 10, the interposed library includes functions 144A, such as bind( ), listen( ), and accept( ), having some of the same names as the functions 144 contained in the OS's network library 142. Since the interposed library is linked to the back end server with a higher precedence than the OS's library, if the back end server calls a named OS function 144 for which there is a similarly named interposed library function 144A, the call will be intercepted by the interposed library function. This means the back end server process's program control will go to the interposed library function 144A, rather than to the similarly named OS function 144.

As shown above, Dukach specifically discloses, teaches and suggests that the interprocess communication links are pipes. Indeed Dukach discloses, teaches and suggests that "interprocess communication links" and "pipes" are identical terms by reciting "**interprocess communication links, or pipes...**" Consequently, Applicants respectfully submit that Dukach specifically discloses, teaches and suggests that pipes are the only form of interprocess communication link suitable for use with Dukach's structure and that Dukach specifically rules out, and teaches away from, the use of any other form of interprocess communication link.

Pipes, such as those specifically disclosed and taught in Dukach, are discussed in the "BACKGROUND OF THE INVENTION SECTION" of Applicants Specification at, for example page 2, line 18 to page 3, line 7. Pipes, such as those specifically

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disclosed and taught in Dukach, are also shown in Applicants FIG.1, clearly marked a "Prior Art". Page 2, line 18 to page 3, line 7 of Applicants Specification reads as follows, with emphasis added:

> Interprocess communication (IPC) is the exchange of data between two or more processes. **Various forms of IPC exists: pipes, sockets, shared memory, message queues, and Solaris ™ doors.**
>
> **A pipe provides the ability for a byte of data to flow in one direction and is used between processes. These two processes must be of common ancestry.** Typically, a pipe is used to communicate between two processes such that the output of one process becomes the input of another process. FIG. 1 illustrates a conventional pipe 100 according to a prior art. The output of process 102 becomes the input of process 104. Pipe 100 is terminated when process 102 that is referencing it terminates. Data is moved from process 102 to process 104 through a pipe 100 situated within a kernel 106.

As shown above, Applicants clearly distinguish pipes as distinct from doors and then explain some of the limitations of pipes. As noted above, the Examiner then goes on to state that Dukach teaches :

> **a door interprocess communication (file descriptor, col 3, ln 62-64/col 10, ln 33-34/ln 53-55), said door interprocess mechanism enabling each process to communication (col 15, ln1-6/col 16, ln 15-21)**

Page 5 lines 3 to 11 of Applicants' Specification reads as follows:

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> **The fastest form of IPC on Solaris™ Operating System from Sun Microsystems Inc. is *doors*. However, applications that want to communicate using *doors* need to be explicitly programmed to do so.** Even though *doors* IPC is very fast, the socket-based IPC is more popular since it is portable, flexible, and can be used to communicate across a network.
>
> A definite need exists for a fast IPC technology that would overcome the drawbacks of *doors* and socket-based IPC. **Specifically, a need exists for a fast socket technology implementation using *doors*.** A primary purpose of the present invention is to solve these needs and provide further, related advantages.

In light of the discussion above, Applicants respectfully submit that, contrary to the Examiners' comments, the disclosure of a "file descriptor" in the Dukach reference is not a disclosure, teaching or suggestion of the "doors" recited in Applicants Claims 1, 7, and 21.

In addition, Dukach fails to disclose, teach or suggest the use of an interposer or interposition as recited in Applicants Claims 1, 7, 13 and 21, as amended.

Applicants further submit that the addition of the Woodring et al reference does nothing to cure these basic deficiencies of the Dukach et al reference. Consequently, Applicants respectfully submit that the Examiner has failed to show where in the Dukach et al reference, Woodring et al reference, or any proper combination of the Dukach et al reference and Woodring et al reference, it is disclosed, taught or suggested a door interprocess communication mechanism, said door interprocess mechanism enabling each process to communicate a synchronization signal or an interposer/interposition mechanism.

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In light of the discussion above, Applicants respectfully request the Examiner withdraw the rejection of Claims 1, 7, 13 and 21 under 35 U.S.C. 103(a) and allow Claims 1, 7, 13 and 21 to issue.

Claims 2 to 6 depend, directly or indirectly on Claim 1, as amended. Consequently Claims 2 to 6 include all of the features of Claim 1, as amended. Claims 8 to 12 depend, directly or indirectly on Claim 7, as amended. Consequently Claims 8 to 12 include all of the features of Claim 7, as amended. Claims 14 to 20 depend, directly or indirectly on Claim 13. Consequently Claims 14 to 20 include all of the features of Claim 13. Therefore, Applicants respectfully request the Examiner withdraw the rejection of Claims 2 to 6, 8 to 12 and 14 to 20 under 35 U.S.C. 103(a) and allow Claims 2 to 6, 8 to 12 and 14 to 20 to issue

CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 19, 2005.

Attorney for Applicant(s) — April 19, 2005 Date of Signature

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